## REMARKS

Claims 1-14 and 16-30 are pending. The Examiner is maintaining the rejection of claims 1-14 and 16-30 under 35 U.S.C. 102(b) as being unpatentable over Normoyle (5,892,957).

In the previous Office Action Response, the Applicants' representative argued that Normoyle does not teach or suggest any delay introduced by a secondary or slave component. Furthermore, Normoyle does not teach or suggest any delay introduced by a secondary or slave component when responding to a primary component request. For example, Normoyle describes "the randomness of the period of time that the master waits before resending an INT request helps to prevent situations where a given interrupt repeatedly sends interrupts to another device." (column 22, lines 47-50) Normoyle also describes a primary component delaying an interrupt to another primary component. "Hence the delayed retry of the interrupt transaction by the interrupter, especially when it is a processor generating the interrupt to another processor, does not violate any processor memory models." (Summary) Sometimes a master component delays processing of a request from a slave component, but this type of delay is different from the typical Normoyle delay as it is not pseudo random. Plus this delay is still master component delay. "Some such possible constraints relate to delaying the processing of a memory or slave request by a given master until any requests to any other memory or slave, respectively, by that same master are resolved." (Figure 3A Description) Normoyle is not believed to describe any slave or secondary component pseudo randomly delaying a response to a primary component.

Although the claims are believed allowable, various claims have been amended to facilitate prosecution. More specifically, independent claims 1 and 28 have been amended to recite "determining a pseudo-random delay at the secondary component prior to responding to the request" and "sending a response from the secondary component after the pseudo-random delay." The amendments to claims 1 and 28 are believed supported by the specification and introduce no new matter. For example, "a system containing multiple primary components and pseudo-randomly delayed (on the basis wait-state/latency/both) secondary components may be used to test many aspects of the arbitration logic rapidly and efficiently. Note that the "tasks" which the primary components execute can be quite simple, without sacrificing test coverage. For example, two primary components may vie for read access to a single pseudo-random wait and pseudo-random latency secondary component. The random delays imposed by the secondary component, syncopating with the requests of the primary components, will tend to

cycle the arbitration logic through substantially all possible interaction configurations, rather than settling into a regular pattern that would exercise only a limited number of interaction configurations." (page 17, lines 21-31) Figures 4 and 5 also show a delay mechanism in a secondary component.

The Examiner acknowledges that it is the system controller and not the secondary component that issues the negative acknowledgement response, but argues that the negative acknowledgement response is "initiated" by the secondary component because the secondary component can not receive the interrupt request. However, the claims have been amended to specifically recite "determining a pseudo-random delay at the secondary component prior to responding to the request" and "sending a response from the secondary component after the pseudo-random delay." None of the references cited by the Examiner either alone or in combination is believed to teach or suggest independent claims 1 and 28.

Independent claims 13 and 21 have been amended to recite "wherein the values include a first value used to adjust the wait-state of the secondary component and a second value used to adjust the latency of the secondary component, wherein the wait-state is time the primary component has to wait before the second component accepts requests and the latency is time the secondary component takes to respond to the request." This amendment is believed supported in the specification and does not introduce any new matter. For example, "As will be discussed below, the delay mechanism may be implemented to adjust the wait-state and/or latency associated with secondary component responses. Generally, wait-state is the time the primary component has to wait before a secondary component will accept its request. Latency is the time the secondary component takes to satisfy the request. Therefore, a system containing multiple primary components and pseudo-randomly delayed (on the basis wait-state/latency/both) secondary components may be used to test many aspects of the arbitration logic rapidly and efficiently." (page 7, lines 17-24) None of the references cited by the Examiner either alone or in combination is believed to teach or suggest independent claims 13 and 21.

## CONCLUSION

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicant's representative believes that all pending claims are allowable in their present form. If the Examiner has any questions, concerns, or remaining issues for Applicant's representative, the Examiner is encouraged to contact her at the number provided below.

Respectfully submitted,
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